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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,875	06/20/2003	Blaine Stackhouse	200207083-1	6673

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EXAMINER	
NGUYEN, DANG T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 10/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,875	STACKHOUSE ET AL.	
	Examiner	Art Unit	
	Dang T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-20,26 and 27* is/are allowed.

6)☒ Claim(s) *1,3-8,11 and 21-25* is/are rejected.

7)☒ Claim(s) *2,9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *Search history*.

Response to Arguments

1. In view of the Appeal Brief filed on 7/06/2006, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

2. Claims 1-27 are pending on this application. Claims 1, 6, 12, 17, 21, 26, and 27 are independent claims.

3. Claims 1, 3-8, 11, and 21-25 of the last office action under 102(b) rejection over prior art Patel et al. are withdrawn.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 6, 8, 21, 22, 24, and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Kotra, U.S. Patent No. US 6,518,809 B1 - filed Aug. 1, 2001.

Regarding independent claim 1, Fig. 2 of Kotra discloses a bias generator (the circuit of Fig. 2) [[for testing of a static random access memory SRAM]] comprising: an output of the bias generator ([PRE-DRIVER_OUTPUT] is output of the bias generator) (*Bias generator defined as a device generate a voltage level to drive other elements, see Webster's Dictionary*); and means [MP2 and MN2] for adjusting a set of available magnitudes of a bias voltage output signal ([PRE-DRIVER OUTPUT] is adjusted, Column 1, lines 64-66) at the output using metal programming (Column 1, lines 66-67).

Even though Kotra does not disclose testing of a SRAM, this limitation has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F .2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F .2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Regarding dependent claim 3, Fig. 2 of Kotra discloses wherein the means for adjusting comprises a metal-programmable transistor [MP2 and MN2] in the bias generator (the circuit of Fig. 2), the metal-programmable transistor [MP2 and MN2] comprising either or both of a metal-programmable pull-up transistor [MP2] and a metal-

programmable pull-down transistor [MN2] that change one or both of a range and a resolution of the set of available magnitudes [PRE-DRIVER_OUTPUT] when the metal-programmable transistors [MP2 and MN2] is metal programmed (Column 1, lines 66-67).

Regarding dependent claim 6, Fig. 2 of Kotra discloses a bias generator (the circuit of Fig. 2) [[for testing of a static random access memory SRAM]] comprising: a metal programmable transistor ([MP2], column 1, lines 65-67) that adjusts a set of available magnitudes of a bias voltage output signal ([PRE-DRIVER_OUTPUT], column 1, lines 64-65) at the bias generator output ([PRE-DRIVER_OUTPUT] is output of the bias generator, Fig. 2) when metal programmed (column 1, lines 66-67).

Regarding dependent claim 8, Kotra discloses the bias generator of claim 6, wherein the metal-programmable transistor comprises either or both of a metal-programmable pull-up transistor [MP2] and a metal-programmable pull-down transistor [MN2], the metal-programmable transistor changing one or both of a range and a resolution of the set of available magnitudes when metal programmed (Col. 1 lines 57-67).

Regarding dependent claim 21, Fig. 2 of Kotra discloses a method of modifying a set of available magnitudes of a bias voltage output signal [PRE-DRIVER_OUTPUT] generated by a bias generator (the circuit of Fig. 2) comprising: providing a metal-programmable transistor [MP2 or MN2] in the bias generator (the circuit of Fig. 2); and metal programming (Column 1 lines 66-67) the metal-programmable transistor [MP2 or MN2] to connect the transistor to circuitry of the bias generator (the circuit of Fig. 2)

such that a corresponding ON state resistance of the metal-programmed transistor [MP2] is combined with an effective ON state resistance of the circuitry [20] to modify the available magnitudes of the set (Column 1, lines 57 – 67).

Regarding dependent claim 22, Fig. 2 of Kotra discloses the method of modifying of claim 21, wherein providing a metal-programmable transistor [MP2 or MN2] comprises providing either or both of a metal-programmable pull-up transistor [MP2] and a metal-programmable pull-down transistor [MN2] in the bias generator (the circuit of Fig. 2), and

wherein metal programming (Column 1 lines 66-67) the metal-programmable transistor [MP2 or MN2] comprises connecting either or both of the metal-programmable pull-up transistor [MP2] and the metal-programmable pull-down transistor [MN2] to the bias generator circuitry (the circuit of Fig. 2).

Regarding dependent claim 24, Fig. 2 of Kotra discloses the method of modifying of Claim 22, wherein metal programming (Column 1 lines 66-67) the metal-programmable pull-down transistor [MN2] to connect to the circuitry (the circuit of Fig. 2) combines a corresponding pull-down ON state resistance of the metal-programmed pull-down transistor [MN2] with an ON state resistance of a of a pull-down transistor [MN1] of the bias generator circuitry (the circuit of Fig. 2).

Regarding dependent claim 25, Fig. 2 of Kotra discloses wherein providing a metal programmable transistors [MP2 or MN2] comprises providing either or both of a selection of metal-programmable pull-up transistors [MP2] and a selection of metal-programmable pull-down transistors [MN2] in the bias generator (the circuit of Fig. 2), at

least one of the metal-programmable transistors [MP2] of each respective selection being different from other metal-programmable transistors [MN2] of the respective selections, and wherein metal programming (column 1 lines 66-67) the metal-programmable transistor [MP2 or MN2] comprises selecting a respective metal-programmable transistor [MP2 or MN2] from either or both the pull-up transistor [MP2] selection and the pull-down transistor [MN2] selection, and connecting the selected respective metal-programmable transistor [MP2 or MN2] to the bias generator circuitry (the circuit of Fig. 2).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-5, 7, 11 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable by Kotra, U.S. patent No. 6,025,737 in view of Patel et al., U.S. patent No. 6,025,737 – filed: Mar. 22, 2002.

Kotra as applied to claims 3, 6 and 22 above disclosed every aspect of applicant's claimed invention except for further comprising: a pull-up array of transistors connected between a first supply voltage and the bias generator output; a pull-down transistor connected between the bias generator output and a second supply voltage;

and a gate circuit connected between a mode select input and a gate of the pull-down transistor, wherein the metal-programmable pull-up transistor is connectable in parallel or in series with the pull-up transistor array, and wherein the metal-programmable pull-down transistor is connectable in parallel or in series with the pull-down transistor; and wherein each of the metal programmable pull-up transistor and the metal-programmable pull-down transistor has a respective ON state resistance that, when either or both are metal programmed, combines with an effective ON state resistance of the pull-up transistor array and an ON state resistance of the pull-down transistor to adjust the set of available magnitudes; and wherein the pull-up array transistors are p-type metal oxide semiconductor (PMOS) transistors that function to pull up the bias voltage output signal when in an ON state, and wherein the pull-down transistor is an n-type metal oxide semiconductor (NMOS) transistor that functions to pull down the bias voltage output signal to the second supply voltage when in the ON state, the second supply voltage being less than the first supply voltage, the second supply voltage optionally being zero volts or a ground voltage.

Fig. 10C of Patel discloses a pull-up array transistors [1062....] connected between a first supply voltage (Fig. 10B [VCCQ]) and the bias generator output [To Core].

a pull-down transistor [1066....] connected between the bias generator output [To Core] and a second supply voltage [GROUND]; and a gate bias circuit (Fig. 10E [shift trip point down]) connected between a mode select input (Fig. 10E [Pin]) and a gate of the pull-down transistor [1064], wherein the metal-programmable pull-up transistor

[1060] is connectable in parallel or in series with the pull-up transistor array [1062 ...], and wherein the metal-programmable pull-down transistor [1064] is connectable in parallel or in series with the pull-down transistor [1066 ....].

Fig. 10C of Patel et al. discloses wherein each of the metal-programmable pull-up transistor [1060] and the metal-programmable pull-down transistor [1064] has a respective ON state resistance that, when either or both are metal programmed, combines with an effective ON state resistance of the pull-up transistor array and an ON state resistance of the pull-down transistor [Figs. 10B, 10D and 10E] to adjust the set of available magnitudes (Col. 15 lines 47-51).

Fig. 10C of Patel discloses wherein the pull-up array transistors are p- type metal oxide semiconductor transistors [1062....] that function to pull up [VCCQ] the bias voltage output signal [To Core] when in an ON state (Fig. 10), and wherein the pull-down transistor is an n-type metal oxide semiconductor transistors [1066 ....] that functions to pull down the bias voltage output signal to the second supply voltage [Ground] when in the ON state (Fig. 10E), the second supply voltage [Ground] being less than the first supply voltage [VCCQ], the second supply voltage optionally being zero volts or a ground voltage [Ground].

Kotra and Patel are common subject matter for metal programming. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated Patel's pull-up array transistors into the bias generator of Kotra for the purpose of providing the manufacturer with the flexibility to chose the

market to support with a minimum cost and the shortest time to market (Col. 1 lines 65-67).

Allowable Subject Matter

6. Claims 2, 9, and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With regard to claim 2, the prior art of record fails to anticipate or make obvious a bias generator for testing of a static random access memory (SRAM), comprising: "wherein the bias voltage output signal biases a gate of a weak write pull-down transistor of a write driver in SRAM with a target magnitude predetermined for the SRAM".

With regard to claim 9, the prior art of record fails to anticipate or make obvious a bias generator for testing of a static random access memory (SRAM), in combination with other limitations, comprising: "wherein the mode select input controls a selection between a weak write test mode (WWTM) and a default mode of operation of the bias generator, and wherein the set of selection inputs selects the set of available magnitudes of the bias voltage output signal in the WWTM, the bias voltage output signal being a logic high level at the bias generator output in the default mode".

With regard to claim 10, the prior art of record fails to anticipate or make obvious a bias generator for testing of a static random access memory (SRAM), in combination with other limitations, comprising: "wherein the mode select input and the

inverse mode select input control a selection between a weak write test mode (WWTM) and a default mode of operation of the bias generator, a set of selection inputs selecting the set of available magnitudes of the bias voltage output signal in the WWTM, the bias voltage output signal being a logic low level at the bias generator output in the default mode".

7. Claims 12 – 20, 26 and 27 are allowed.

The following is an examiner's statement of reasons for allowance:

With regard to claim 12, the prior art of record fails to anticipate or make obvious a metal-programmable weak write test mode (MPWWTM) bias generator for weak write test mode (WWTM) testing of a static random access memory (SRAM), in combination with other limitations, comprising: "wherein the mode select input controls a selection between a WWTM and a default mode of operation of the MPWWTM bias generator, a set of selection inputs selecting the set of available magnitudes of the bias voltage output signal in the WWTM, the bias voltage output signal being a logic high level at the MPWWTM bias generator output in the default mode".

With regard to claim 17, the prior art of record fails to anticipate or make obvious a metal-programmable weak write test mode (MPWWTM) bias generator for weak write test mode (WWTM) testing of a static random access memory (SRAM), in combination with other limitations, comprising: "a first transistor having a source connected to drains of the transistors of the pull-up array, a drain connected to the MPWWTM bias generator output; and a second transistor having a source connected to the second supply voltage, a drain connected to the MPWWTM bias generator output,

and a gate connected to the inverse mode select input; and wherein the mode select input and the inverse mode select input control a selection between a WWTM and a default mode of operation of the MPWWTM bias generator, a set of selection inputs selecting the set of available magnitudes of the bias voltage output signal in the WWTM, the bias voltage output signal being a logic low level at the MPWWTM bias generator output in the default mode".

With regard to claim 26, the prior art of record fails to anticipate or make obvious a bias generator for testing of a static random access memory (SRAM), in combination with other limitations, comprising: " wherein the mode select input controls a selection between a weak write test mode (WWTM) and a default mode of operation of the bias generator, and wherein the set of selection inputs selects the set of available magnitudes of the bias voltage output signal in the WWTM, the bias voltage output signal being a logic high level at the bias generator output in the default mode".

With regard to claim 27, the prior art of record fails to anticipate or make obvious a bias generator for testing of a static random access memory (SRAM), in combination with other limitations, comprising: "wherein the mode select input and the inverse mode select input control a selection between a weak write test mode (WWTM) and a default mode of operation of the bias generator, a set of selection inputs selecting the set of available magnitudes of the bias voltage output signal in the WWTM, the bias voltage output signal being a logic low level at the bias generator output in the default mode".

Dependent claims 13 - 16 and 18 - 20 are allowed based on independent claims 12 and 17 above.

Prior art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lee Patent No. US 6,356,139 B1 Date of Patent: Mar. 12, 2002

Contact Information

9. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 10/13/2006

Conferees:

Richard Elms

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Anh Phung 10/16/06

ANH PHUNG
PRIMARY EXAMINER